WHAT IS CLAIMED IS

1. A display device comprising:

a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column;

a monitor line held at a first potential;

a control circuit for generating at least a clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of the monitor line, and correcting the timings of generation of at least said clock signal and inverse clock signal based on the change of the timing of the potential change;

a horizontal scanner; and

a monitor circuit, wherein

said horizontal scanner includes:

a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first

scanning operation or the time of said second scanning operation,

a first switch group for alternately sequentially sampling said clock signal and inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion, and

said monitor circuit includes:

a selector portion for receiving said switch signal, sampling signals different from the signal sampled by the first shift stage of the shift register in said horizontal scanner among said clock signal and inverse clock signal when the switch signal indicates said first scanning operation and sampling signals different from the signal sampled by the last shift stage of the shift register in said horizontal scanner among said clock signal and inverse clock signal when the switch signal indicates said second scanning operation, and outputting the same as the sample-and-hold pulses, and

a third switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said selector portion.

2. A display device as set forth in claim 1, wherein said selector portion comprises:

a fourth switch for receiving a select pulse and sampling said clock signal and outputting the same as the sample-and-hold pulse to said third switch,

a fifth switch for receiving said select pulse and sampling said inverse clock signal and outputting the same as the sample-and-hold pulse to said third switch, and

a selector for receiving said switch signal, outputting said select pulse to said fourth switch when the switch signal indicates said first scanning operation, and outputting said select pulse to said fifth switch when the switch signal indicates said second scanning operation.

3. A display device as set forth in claim 2, wherein:

said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, the horizontal start pulse is supplied to the initial shift stage of said shift register and said monitor circuit at the time of said

first scanning operation, supplied to the last shift stage of said shift register and said monitor circuit at the time of said second scanning operation, and

the selector of said monitor circuit supplies said horizontal start pulse as said select pulse to said fourth switch or fifth switch in accordance with said switch signal.

4. A display device as set forth in claim 3, wherein said selector comprises:

a first transfer line for transferring said horizontal start pulse as said select pulse to said fourth switch,

a second transfer line for transferring said horizontal start pulse as said select pulse to said fifth switch,

a first select switch for connecting said first transfer line to the supply line of said horizontal start pulse when said switch signal indicates said first scanning operation,

a second select switch for connecting said second transfer line to the supply line of said horizontal start pulse when said switch signal indicates said second scanning operation, and

a potential setting means for retaining said first transfer line or said second transfer line in a

nonconnection state with the supply line of said horizontal start pulse at a potential able to hold said fourth switch or said fifth switch to which the first transfer line or said second transfer line is connected in a nonconductive state.

5. A display device as set forth in claim 1, wherein the number of the shift stages in the shift register of said horizontal scanner is even.

6. A display device as set forth in claim 2, further comprising:

a clock generating means for generating, based on the clock signal and the inverse clock signal generated at said control circuit, a second clock signal and a second inverse clock signal having the same period as the clock signal and inverse clock signal and having a small duty ratio and supplying the same to said horizontal scanner and monitor circuit, and wherein

each switch of the first switch group of said horizontal scanner and the fourth switch or the fifth switch of said monitor circuit samples the second clock signal or second inverse clock signal from said clock generating means.

7. A display device as set forth in claim 1, wherein the display element of said pixels is a liquid crystal cell.

8. A display device comprising:

a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column;

a monitor line held at a first potential;

a control circuit for generating at least a first clock signal and a first inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of said monitor line, and correcting the timings of generation of at least said clock signal and inverse clock signal based on the change of the timing of the potential change;

a clock generation circuit for generating a second clock signal and a second inverse clock signal having the same period as the first clock signal and first inverse clock signal and having a small duty ratio based on said first clock signal and first inverse clock signal generated at said control circuit;

a horizontal scanner; and

a monitor circuit, wherein

said horizontal scanner includes:

a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially

shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first scanning operation or the time of said second scanning operation,

a first switch group for alternately sequentially sampling said second clock signal and second inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion, and

said monitor circuit includes:

a selector portion for receiving said switch signal, sampling signals having different phases from that of the signal sampled by the first shift stage of the shift register in said horizontal scanner between said first clock signal and first inverse clock signal

when the switch signal indicates said first scanning operation and sampling signals having different phases from that of the signal sampled by the last shift stage of the shift register in said horizontal scanner between said first clock signal and first inverse clock signal when the switch signal indicates said second scanning operation, and outputting the same as the sample-and-hold pulses, and

a third switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said selector portion.

9. A display device as set forth in claim 8, wherein said selector portion comprises:

a fourth switch for receiving a select pulse and sampling said clock signal and outputting the same as the sample-and-hold pulse to said third switch,

a fifth switch for receiving said select pulse and sampling said inverse clock signal and outputting the same as the sample-and-hold pulse to said third switch, and

a selector for receiving said switch signal, outputting said select pulse to said fourth switch when the switch signal indicates said first scanning operation, and outputting said select pulse to said fifth switch when the switch signal indicates said second scanning

operation.

10. A display device as set forth in claim 9, wherein:

said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, the horizontal start pulse is supplied to the initial shift stage of said shift register and said monitor circuit at the time of said first scanning operation, supplied to the last shift stage of said shift register and said monitor circuit at the time of said second scanning operation, and

the selector of said monitor circuit supplies said horizontal start pulse as said select pulse to said fourth switch or fifth switch in accordance with said switch signal.

11. A display device as set forth in claim 10, wherein said selector has:

a first transfer line for transferring said horizontal start pulse as said select pulse to said fourth switch,

a second transfer line for transferring said horizontal start pulse as said select pulse to said fifth switch,

a first select switch for connecting said first transfer line to the supply line of said horizontal start

pulse when said switch signal indicates said first scanning operation,

a second select switch for connecting said second transfer line to the supply line of said horizontal start pulse when said switch signal indicates said second scanning operation, and

a potential setting means for retaining said first transfer line or said second transfer line in a nonconnection state with the supply line of said horizontal start pulse at a potential able to hold said fourth switch or said fifth switch to which the first transfer line or said second transfer line is connected in a nonconductive state.

12. A display device as set forth in claim 8, wherein the number of the shift stages in the shift register of said horizontal scanner is even.

13. A display device as set forth in claim 8, wherein the display element of said pixels is a liquid crystal cell.

14. A display device comprising:

a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column;

a monitor line held at a first potential;

a control circuit for generating at least a

clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of said monitor line, and correcting the timings of generation of at least said clock signal and inverse clock signal based on the change of the timing of the potential change;

a horizontal scanner;

a first monitor circuit; and

a second monitor circuit, wherein

said horizontal scanner includes:

a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first scanning operation or the time of said second scanning operation,

a first switch group for alternately sequentially sampling said clock signal and inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and

outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion,

said first monitor circuit includes:

a shift stage which is connected to the last shift stage of the shift register in said horizontal scanner at the time of said first scanning operation and outputs the shift pulses in synchronization with said clock signal and inverse clock signal when performing shift-in of the signal by the last shift stage,

a third switch for sampling signals different from the signal sampled from said last shift stage among said clock signal and inverse clock signal in response to said shift pulse output from said shift stage and outputting the same as the sample-and-hold pulses, and

a fourth switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said third switch, and

said second monitor circuit includes:

a shift stage which is connected to the initial shift stage of the shift register in said horizontal scanner at the time of said second scanning operation and

outputs the shift pulses in synchronization with said clock signal and inverse clock signal when performing the shift-in of the signal by the initial shift stage,

a fifth switch for sampling signals different from that of the signal sampled from said initial shift stage among said clock signal and inverse clock signal in response to said shift pulses output from said shift stage and outputting the same as the sample-and-hold pulses, and

a sixth switch for setting the potential of said monitor line at the second potential in response to the sample-and-hold pulses from said fifth switch.

15. A display device as set forth in claim 14, wherein said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, and the horizontal start pulse is supplied to the initial shift stage of said shift register at the time of said first scanning operation, supplied to the last shift stage of said shift register at the time of said second scanning operation, and not supplied to said first monitor circuit and said second monitor circuit.

16. A display device as set forth in claim 14, wherein:

said first monitor circuit is arranged in the

vicinity of the arrangement position of the last shift stage of said horizontal scanner, and

said second monitor circuit is arranged in the vicinity of the arrangement position of the initial shift stage of said horizontal scanner.

17. A display device as set forth in claim 14, wherein said monitor line is shared by said first monitor circuit and said second monitor circuit.

18. A display device as set forth in claim 14, wherein said monitor line is individually formed as a first monitor line connected to said first monitor circuit and as a second monitor line connected to said second monitor circuit.

19. A display device as set forth in claim 14, wherein the number of shift stages in the shift register of said horizontal scanner is even.

20. A display device as set forth in claim 14, further comprising:

a clock generating means for generating, based on the clock signal and the inverse clock signal generated at said control circuit, a second clock signal and a second inverse clock signal having the same period as the clock signal and inverse clock signal and having a small duty ratio and supplying the same to said horizontal scanner, first monitor circuit, and the second

monitor circuit, and wherein

each switch of the first switch group of said horizontal scanner, the third switch of said first monitor circuit, and the fifth switch of said second monitor circuit samples the second clock signal or second inverse clock signal from said clock generating means.

21. A display device as set forth in claim 14, wherein the display element of said pixels is a liquid crystal cell.

22. A projection type display device comprising:

a monitor line held at a first potential;

a control circuit for generating at least a clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of said monitor line, and correcting at least the timings of generation of said clock signal and inverse clock signal based on the change of the timing of the potential change;

a display panel including a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column, a horizontal scanner, and a monitor circuit;

an irradiating means for irradiating the light to said display panel; and

a projecting means for projecting light passing through said display panel, wherein

the horizontal scanner of said display panel includes:

a shift register in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first scanning operation or the time of said second scanning operation,

a first switch group for alternately sequentially sampling said clock signal and inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion, and

the monitor circuit of said display panel includes:

a selector portion for receiving said switch signal, sampling signals different from the signal sampled by the first shift stage of the shift register in said horizontal scanner among said clock signal and inverse clock signal when the switch signal indicates said first scanning operation and sampling signals different from the signal sampled by the last shift stage of the shift register in said horizontal scanner among said clock signal and inverse clock signal when the switch signal indicates said second scanning operation, and outputting the same as the sample-and-hold pulses, and

a third switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said selector portion.

23. A projection type display device as set forth in claim 22, wherein said selector portion comprises:

a fourth switch for receiving select a pulse and sampling said clock signal and outputting the same as the sample-and-hold pulse to said third switch,

a fifth switch for receiving said select pulse and sampling said inverse clock signal and outputting the same as the sample-and-hold pulse to said third switch,

and

a selector for receiving said switch signal, outputting said select pulse to said fourth switch when the switch signal indicates said first scanning operation, and outputting said select pulse to said fifth switch when the switch signal indicates said second scanning operation.

24. A projection type display device as set forth in claim 23, wherein:

said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, the horizontal start pulse is supplied to the initial shift stage of said shift register and said monitor circuit at the time of said first scanning operation, supplied to the last shift stage of said shift register and said monitor circuit at the time of said second scanning operation, and

the selector of said monitor circuit supplies said horizontal start pulse as said select pulse to said fourth switch or fifth switch in accordance with said switch signal.

25. A projection type display device as set forth in claim 24, wherein said selector comprises:

a first transfer line for transferring said horizontal start pulse as said select pulse to said

fourth switch,

a second transfer line for transferring said horizontal start pulse as said select pulse to said fifth switch,

a first select switch for connecting said first transfer line to the supply line of said horizontal start pulse when said switch signal indicates said first scanning operation,

a second select switch for connecting said second transfer line to the supply line of said horizontal start pulse when said switch signal indicates said second scanning operation, and

a potential setting means for retaining said first transfer line or said second transfer line in a nonconnection state with the supply line of said horizontal start pulse at a potential able to hold said fourth switch or said fifth switch to which the first transfer line or said second transfer line is connected in a nonconductive state.

26. A projection type display device as set forth in claim 22, wherein the number of the shift stages in the shift register of said horizontal scanner is even.

27. A projection type display device as set forth in claim 23, further comprising:

provision is made of a clock generating means

for generating, based on the clock signal and the inverse clock signal generated at said control circuit, a second clock signal and a second inverse clock signal having the same period as the clock signal and inverse clock signal and having a small duty ratio and supplying the same to said horizontal scanner and monitor circuit, and wherein

each switch of the first switch group of said horizontal scanner and the fourth switch or the fifth switch of said monitor circuit samples the second clock signal or second inverse clock signal from said clock generating means.

28. A projection type display device as set forth in claim 22, wherein the display element of said pixels is a liquid crystal cell.

29. A projection type display device comprising:

a monitor line held at a first potential;

a control circuit for generating at least a clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of said monitor line, and correcting at least the timings of generation of said clock signal and inverse clock signal based on the change of the timing of the potential change;

a clock generation circuit for generating a

second clock signal and a second inverse clock signal having the same period as the first clock signal and first inverse clock signal and having a small duty ratio based on said first clock signal and first inverse clock signal generated at said control circuit;

a display panel including at least a pixel portion in which a plurality of pixels are arrayed in a matrix and signal lines are laid for every pixel column, a horizontal scanner, and a monitor circuit;

an irradiating means for irradiating light to said display panel; and

a projecting means for projecting the light passed through said display panel onto a screen, wherein

the horizontal scanner of said display panel includes:

a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first scanning operation or the time of said second scanning

operation,

a first switch group for alternately sequentially sampling said second clock signal and second inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion, and

the monitor circuit of said display panel includes:

a selector portion for receiving said switch signal, sampling signals having different phases from that of the signal sampled by the first shift stage of the shift register in said horizontal scanner between said first clock signal and first inverse clock signal when the switch signal indicates said first scanning operation and sampling signals having different phases from that of the signal sampled by the last shift stage of the shift register in said horizontal scanner between said first clock signal and first inverse clock signal when the switch signal indicates said second scanning

operation, and outputting the same as the sample-and-hold pulses, and

a third switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said selector portion.

30. A projection type display device as set forth in claim 29, wherein said selector portion comprises:

a fourth switch for receiving a select pulse and sampling said clock signal and outputting the same as the sample-and-hold pulse to said third switch,

a fifth switch for receiving said select pulses and sampling said inverse clock signal and outputting the same as the sample-and-hold pulse to said third switch, and

a selector for receiving said switch signal, outputting said select pulse to said fourth switch when the switch signal indicates said first scanning operation, and outputting said select pulse to said fifth switch when the switch signal indicates said second scanning operation.

31. A projection type display device as set forth in claim 30, wherein:

said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, the horizontal start pulse is

supplied to the initial shift stage of said shift register and said monitor circuit at the time of said first scanning operation and supplied to the last shift stage of said shift register and said monitor circuit at the time of said second scanning operation, and

the selector of said monitor circuit supplies said horizontal start pulse as said select pulse to said fourth switch or fifth switch in accordance with said switch signal.

32. A projection type display device as set forth in claim 31, wherein said selector comprises:

a first transfer line for transferring said horizontal start pulse as said select pulse to said fourth switch,

a second transfer line for transferring said horizontal start pulse as said select pulse to said fifth switch,

a first select switch for connecting said first transfer line to the supply line of said horizontal start pulse when said switch signal indicates said first scanning operation,

a second select switch for connecting said second transfer line to the supply line of said horizontal start pulse when said switch signal indicates said second scanning operation, and

a potential setting means for holding said first transfer line or said second transfer line in a nonconnection state with the supply line of said horizontal start pulse at a potential able to hold said fourth switch or said fifth switch to which the first transfer line or said second transfer line is connected in a nonconductive state.

33. A projection type display device as set forth in claim 29, wherein the number of the shift stages in the shift register of said horizontal scanner is even.

34. A projection type display device as set forth in claim 29, wherein the display element of said pixels is a liquid crystal cell.

35. A projection type display device comprising:

a monitor line held at a first potential;

a control circuit for generating at least a clock signal and an inverse clock signal having inverse phases to each other and serving as reference of a horizontal scan, monitoring the potential change of said monitor line, and correcting at least the timings of generation of said clock signal and inverse clock signal based on the change of the timing of the potential change;

a display panel including a pixel portion in which a plurality of pixels are arrayed in a matrix and

signal lines are laid for every pixel column, a horizontal scanner, a first monitor circuit, and a second monitor circuit;

an irradiating means for irradiating light to said display panel; and

a projecting means for projecting the light passed through said display panel onto a screen, wherein

the horizontal scanner of said display panel includes:

a shift register, in which a plurality of shift stages are cascade connected, which is able to switch between a first scanning operation for sequentially shifting from a first stage to a last stage and a second scanning operation for sequentially shifting from the last stage to the first stage in accordance with the switch signal and sequentially outputs shift pulses from the shift stages in synchronization with said clock signal and inverse clock signal at the time of said first scanning operation or the time of said second scanning operation,

a first switch group for alternately sequentially sampling said clock signal and inverse clock signal in response to said shift pulses output from the corresponding shift stages of said shift register and outputting them as sample-and-hold pulses, and

a second switch group for sequentially sampling video signals in response to the sample-and-hold pulses from the switches of said first switch group and supplying them to the corresponding signal lines of said pixel portion,

the first monitor circuit of said display panel includes:

a shift stage which is connected to the last shift stage of the shift register in said horizontal scanner at the time of said first scanning operation and outputs the shift pulses in synchronization with said clock signal and inverse clock signal when performing the shift-in of the signal by the last shift stage,

a third switch for sampling signals different from the signal sampled from said last shift stage among said clock signal and inverse clock signal in response to said shift pulse output from said shift stage and outputting the same as the sample-and-hold pulses, and

a fourth switch for setting the potential of said monitor line at a second potential in response to the sample-and-hold pulses from said third switch, and

the second monitor circuit of said display panel includes:

a shift stage which is connected to the initial shift stage of the shift register in said horizontal

scanner at the time of said second scanning operation and outputs the shift pulses in synchronization with said clock signal and inverse clock signal when performing the shift-in of the signal by the initial shift stage,

a fifth switch for sampling signals different from that of the signal sampled from said initial shift stage among said clock signal and inverse clock signal in response to said shift pulses output from said shift stage and outputting the same as the sample-and-hold pulses, and

a sixth switch for setting the potential of said monitor line at the second potential in response to the sample-and-hold pulses from said fifth switch.

36. A projection type display device as set forth in claim 35, wherein said first scanning operation and said second scanning operation are started by receiving the horizontal start pulse, and the horizontal start pulse is supplied to the initial shift stage of said shift register at the time of said first scanning operation, supplied to the last shift stage of said shift register at the time of said second scanning operation, and not supplied to said first monitor circuit and said second monitor circuit.

37. A projection type display as set forth in claim 35, wherein:

said first monitor circuit is arranged in the vicinity of the arrangement position of the last shift stage of said horizontal scanner, and

said second monitor circuit is arranged in the vicinity of the arrangement position of the initial shift stage of said horizontal scanner.

38. A projection type display device as set forth in claim 35, wherein said monitor line is shared by said first monitor circuit and said second monitor circuit.

39. A projection type display device as set forth in claim 35, wherein said monitor line is individually formed as a first monitor line connected to said first monitor circuit and as a second monitor line connected to said second monitor circuit.

40. A projection type display device as set forth in claim 35, wherein the number of shift stages in the shift
register of said horizontal scanner is even.

41. A projection type display device as set forth in claim 35, further comprising:

a clock generating means for generating, based on the clock signal and the inverse clock signal generated at said control circuit, a second clock signal and a second inverse clock signal having the same period as the clock signal and inverse clock signal and having a

small duty ratio and supplying the same to said horizontal scanner, first monitor circuit, and the second monitor circuit, and wherein

each switch of the first switch group of said horizontal scanner, the third switch of said first monitor circuit, and the fifth switch of said second monitor circuit samples the second clock signal or second inverse clock signal from said clock generating means.

42. A projection type display device as set forth in claim 35, wherein the display element of said pixels is a liquid crystal cell.